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EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/351,544	CARNS ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-11,15-30,36-39 and 72-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-11,15-30,36-39 and 72-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *26 February 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The declaration under 37 CFR 1.132 filed July 30, 2002 is sufficient to overcome the rejection of claims 3 – 11, 15 – 30 and 36 – 42 based upon the previous U.S.C. sections 102 and 103 rejections in the office action filed May 3, 2002 based on Kayanuma and Takahashi because the silicide layers of the references are not the same as the anti-reflective layer claimed.

Drawings

2. The corrected or substitute drawings were received on February 26, 2002. These drawings are approved.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 81 – 85 rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is not clear how one of ordinary skill in the art would optimize process parameters for a step wherein the process parameters can only be determined when a second step is performed without the original step.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 78, 79, and 81 – 85 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear in claim 78 if the "subsequently" clause is defining the same step as the previous "subsequently" clause defined in claim 26, from which claim 78 depends. Is the removing step different than the etching step? Are "more than one capacitors" formed multiple times? For purposes of this office action, the "subsequently" clause in claim 78 will not be considered.

With regard to claim 81, it is not clear if "an optional capacitor process" is performed. The phrase "when the optional capacitor process module is omitted" is not clear because it does not define whether the subsequent claim limitations bear any weight if there is no capacitor process module. How can the step of forming one or more transistors be dependent on a process step that does not exist? What does the "wherein" phrase actually define?

With regard to claim 82, it is not clear if "a dielectric layer" is the same as "a dielectric layer" in claim 81, from which 82 depends. Are there two "a dielectric layers"? For purposes of this office action "a dielectric layer" in claim 82 will be considered --said dielectric layer--. Further it should be noted that it is unclear "forming a top electrode layer" relates to "forming a top capacitor electrode" in claim 81. There should be some reference made to "forming a top

capacitor electrode" in claim 82 before the "forming a top electrode layer" is defined. Still further, how can the "exposed dielectric layer" be "proximate to said exposed dielectric layer"?

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3, 8 – 11, 36, 39, 74, 81 – 83, and 85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi (USPAT 5683931) in view of Bencher et al. ("Dielectric Antireflective coatings for DUV Lithography", Solid State Technology, March 1997, p. 109, Bencher).

With regard to claim 3, Takahashi discloses in figures 2a – 2e forming a capacitor in an integrated circuit. Takahashi discloses in figure 2a forming a bottom electrode layer (304) on a semiconductor body (301). Takahashi discloses in figure 2b forming a dielectric layer (305) over at least a portion of the bottom electrode. Takahashi discloses in figure 2b forming a top electrode layer (306) over at least a portion of the dielectric layer. Takahashi discloses in figure 2c removing a portion of the top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode; and subsequently removing at least a portion of the exposed portion of the dielectric layer to expose a portion of the lower electrode layer, wherein a portion of the dielectric is removed from an intermediate region between the top electrode and the

bottom electrode layer. Takahashi discloses in figure 2d subsequently forming a conformal insulating layer (307) over at least a portion of the exposed portion of the bottom electrode layer proximate to the exposed dielectric layer, the exposed dielectric layer and at least part of the top electrode layer proximate to the exposed dielectric layer, whereby a portion of the conformal insulating layer is formed in the intermediate region. Takahashi discloses in figure 2e etching the bottom electrode layer using a photolithographic mask (309) subsequent to forming the conformal insulating layer. Takahashi is silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the conformal insulating layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher subsequent to forming the conformal insulating layer and before forming the photolithographic mask in the method of Takahashi in order to easily maintain critical dimension (CD) control during pattern transfer in a photolithographic step as stated by Bencher in the last paragraph before the Dielectric ARC Design section.

With regard to claim 8, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the ARL is an anti-reflective coating.

With regard to claim 9, Bencher teaches in the first paragraph after the Dielectric ARC Design section wherein the ARL is titanium nitride.

With regard to claim 10, Bencher teaches in the first sentence of the article wherein the ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

With regard to claim 11, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness of 300 angstroms.

With regard to claim 36, Takahashi discloses in figure 2b forming a conductive layer on a semiconductor body. Takahashi discloses in figure 2c forming a capacitor structure comprising: a top electrode over a portion of the conductive layer; and a dielectric layer between the top electrode and the conductive layer. Takahashi discloses in figure 2d forming a conformal insulating layer over the capacitor structure and at least a portion of the conductive layer proximate to the capacitor structure, whereby a portion of the conformal layer is formed in the region between the top electrode and the conductive layer. Takahashi discloses in figure 2e forming a patterned mask over the structure resultant from the forming a conformal insulating layer. Takahashi is silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the resultant structure resultant from forming the conformal insulating layer before forming the patterned mask. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure before forming a patterned mask. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher on the structure resultant from the forming the conformal insulating layer and before forming the patterned mask in the method of Takahashi in order to easily maintain critical dimension (CD) control during pattern transfer in a photolithographic (patterning the mask) step as stated by Bencher in the last paragraph before the Dielectric ARC

Design section. Takahashi discloses in figure 2e etching the conductive layer using the patterned mask.

With regard to claim 39, Takahashi discloses in figure 2e wherein the conductive layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

With regard to claim 74, Bencher discloses in the Step 2 section under Dielectric ARC Design wherein the anti-reflective layer is a Si_xON_y film.

As far as the examiner can ascertain, Takahashi and Bencher teach the limitations of claims 81 – 83 and 85 similar to claims 3, 8 – 11, 36, and 39 above.

9. Claims 4 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi in view of Bencher and Wang et al. (USPAT 5545585, Wang).

With regard to claim 4, Takahashi discloses in figures 2a – 2e forming a capacitor in an integrated circuit. Takahashi discloses in figure 2a forming a bottom electrode layer (304) on a semiconductor body (301). Takahashi discloses in figure 2b forming a dielectric layer (305) over at least a portion of the bottom electrode. Takahashi discloses in figure 2b forming a top electrode layer (306) over at least a portion of the dielectric layer. Takahashi discloses in figure 2c removing a portion of the top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode; and subsequently removing at least a portion of the exposed portion of the dielectric layer to expose a portion of the lower electrode, wherein a portion of the dielectric layer is removed from an intermediate region between the top electrode and the bottom electrode layer. Takahashi discloses in figure 2d subsequently forming a conformal insulating layer (307) over at least a portion of the exposed portion of the bottom electrode layer proximate

to the exposed dielectric layer, the exposed dielectric layer and at least part of the top electrode layer proximate to the exposed dielectric layer, whereby a portion of the conformal insulating layer is formed in the intermediate region. Takahashi discloses in figure 2e etching the bottom electrode layer using a photolithographic mask (309) subsequent to forming the conformal insulating layer. Takahashi is silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the conformal insulating layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher subsequent to forming the conformal insulating layer and before forming the photolithographic mask in the method of Takahashi in order to easily maintain critical dimension (CD) control during pattern transfer in a photolithographic step as stated by Bencher in the last paragraph before the Dielectric ARC Design section. Takahashi and Bencher are silent to the conformal insulating layer having a thickness in the range of from 20 Å to 70 Å. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Takahashi and Bencher in order to form a material of high dielectric constant that is compatible with ULSI polysilicon processing as stated by Wang in column 1, lines 16 – 17, column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 5, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is an oxide layer is formed in a thermal process.

With regard to claim 6, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the thermal process is a thermal oxidation. Takahashi, Bencher and Wang do not disclose that the conformal insulating layer is formed in a rapid thermal process that is a rapid thermal oxidation performed for a length of time in the range of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C. It is well known in the art to use a rapid thermal process in the production of a thermal oxide layer that has parameters of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use a rapid thermal process that has parameters of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C to form the conformal insulating layer of Takahashi, Bencher and Wang in order to choose a method that is widely used and understood in the art and produces a consistent and reliable oxide layer.

With regard to claim 7, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is formed by deposition.

10. Claims 15, 16, 19 – 25, and are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma et al. (USPAT 5397729, Kayanuma) in view of Segawa et al. (JPPAT 10004179A, Segawa) and Bencher.

In regard to claim 15, Kayanuma discloses in figures 4a – 4f and column 10, lines 38 – 40 forming a capacitor in an integrated circuit. Kayanuma discloses in figure 4a forming a bottom electrode layer (52) on a semiconductor body (50). Kayanuma discloses in figure 4a forming a dielectric layer (53) over at least a portion of the bottom electrode. Kayanuma discloses in figure

4a forming a top electrode layer (54) over at least a portion of the dielectric layer. Kayanuma discloses in figure 4b and column 10, lines 38 – 40 removing a portion of the top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode. Kayanuma discloses in figure 4c and column 10, lines 38 – 40 forming an insulating layer (57) over at least a portion of the top electrode layer and the exposed portion of the dielectric layer. Kayanuma discloses in figure 4d removing a portion of the insulating layer and a portion of the dielectric layer, thereby exposing at least a portion of the lower electrode and forming side wall spacers , wherein the side wall spacers are formed on the side walls of the top electrode and of the inter electrode region of the dielectric. Kayanuma does not teach the removing step wherein the top of the top electrode is exposed. Segawa teaches in figures 1a – 1g removing a portion of an insulating layer and a portion of a dielectric layer, thereby exposing at least a portion of the lower electrode and forming side wall spacers, wherein the side wall spacers are formed on the side walls of the top electrode and of the inter electrode region of the dielectric, and wherein the top of the top electrode is exposed. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the removing step of Segawa in the method of Kayanuma in order to prepare the top surface of the top electrode for an electrical connection as taught by Segawa in figures 1a – 1g. Kayanuma discloses in figures 4d – 4e etching the bottom electrode layer using a photolithographic mask (60) subsequent to removing a portion of the insulating layer.
Kayanuma and Segawa are silent to teaching forming a non-insulating layer over at least a portion of the top electrode, the side wall spacers and the lower electrode layer, wherein the non-insulating layer is an anti-reflective layer (ARL) for use in a photolithographic process. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective

layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the non-insulating layer of Bencher that is an anti-reflective layer for use in a photolithographic step subsequent to removing a portion of the insulating layer and a portion of the dielectric layer and before forming the photolithographic mask in the method of Kayanuma and Segawa in order to easily maintain critical dimension (CD) control during pattern transfer in a photolithographic step as stated by Bencher in the last paragraph before the Dielectric ARC Design section.

With regard to claim 16, Kayanuma discloses in column 8, lines 48 – 52 wherein the insulating layer is formed by deposition.

With regard to claim 19, Kayanuma discloses in column 8, lines 48 – 52 wherein the insulating layer is an oxide layer with a thickness of 1000 Å.

With regard to claim 20, Kayanuma discloses in column 8, lines 33 – 36 and 48 – 52 wherein the side wall spacers have a width in the range of about 1450 Å.

With regard to claim 21, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the ARL is an anti-reflective coating.

With regard to claim 22, Bencher teaches in the first paragraph after the Dielectric ARC Design section wherein the ARL is titanium nitride.

With regard to claim 23, Bencher teaches in the first sentence of the article wherein the ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

With regard to claim 24, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness of 300 angstroms.

With regard to claim 25, Kayanuma discloses in figure 4f wherein the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

With regard to claim 77, Bencher discloses in the Step 2 section under Dielectric ARC Design wherein the anti-reflective layer is a Si_xON_y film.

11. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma, Segawa, and Bencher as applied to claims 15 and 16 above, and further in view of Patel et al. (USPAT 5374578, Patel).

Kayanuma and Bencher do not teach wherein prior to forming the insulating layer by deposition, an anneal is performed. Patel teaches in figures 6 and 7 and column 5, lines 13 – 18 prior to forming an insulating layer (18) by deposition, an anneal is performed. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the anneal of Patel in the method of Kayanuma in order to reduce electrode and material deficiencies as stated by Kayanuma in column 1, lines 13 – 17.

12. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma, Segawa and Bencher as applied to claim 15, above, and further in view of Wang.

With regard to claim 18, Kayanuma and Bencher do not disclose wherein the insulating layer is grown. Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 growing an insulating layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use method of growing an insulating layer of Wang in the method of Kayanuma in order to form a material of high dielectric constant that is compatible with polysilicon processing as stated by Wang in column 7, lines 65 – 67 and column 8, lines 1 – 16.

13. Claims 26 – 30 and 80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma in view of Bencher.

With regard to claim 26, Kayanuma discloses in figures 4d – 4e a method of forming a capacitor in an integrated circuit. Kayanuma discloses in figures 4d – 4e forming a bottom electrode layer (52) on a semiconductor body (50). Kayanuma discloses in figures 4d – 4e forming a dielectric layer (53) over at least a portion of the bottom electrode. Kayanuma discloses in figures 4d – 4e forming a top electrode layer (54) over at least a portion of the dielectric layer. Kayanuma discloses in figures 4d – 4e removing a portion of the top electrode layer to expose a portion of the dielectric layer thereby forming a top electrode, wherein the bottom electrode layer is not exposed. Kayanuma discloses in figures 4d – 4e subsequently forming a photolithographic mask (58) and removing a portion of the exposed portion of the dielectric layer and a portion of the bottom electrode layer, thereby exposing at least a portion of the semiconductor body and forming one or more capacitors. Kayanuma is silent to forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the top electrode and the exposed portion of the dielectric layer before the step of forming the

photolithographic mask. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher before forming the photolithographic mask in the method of Kayanuma in order to easily maintain critical dimension (CD) control during pattern transfer in a photolithographic step as stated by Bencher in the last paragraph before the Dielectric ARC Design section.

With regard to claim 27, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the ARL is an anti-reflective coating.

With regard to claim 28, Bencher teaches in the first paragraph after the Dielectric ARC Design section wherein the ARL is titanium nitride.

With regard to claim 29, Bencher teaches in the first sentence of the article wherein the ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

With regard to claim 30, Kayanuma discloses in figures 4d – 4e wherein the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

With regard to claim 80, Bencher discloses in the Step 2 section under Dielectric ARC Design wherein the anti-reflective layer is a Si_xON_y film.

14. Claims 37, 38 and 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahasi and Bencher as applied to claims 36, 40, 48, 81 and 82 above, and further in view of Wang.

With regard to claim 37 Takahashi and Bencher do not disclose that the conformal insulating layer has a thickness in the range of from 20 Å to 70 Å. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Takahasi and Bencher in order to form a material of high dielectric constant that is compatible with polysilicon processing as stated by Wang in column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 38, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is an oxide layer is formed in a thermal process.

As far as the examiner can ascertain, Takahashi, Bencher and Wang teach the limitation of claim 82 similar to claim 37 above.

15. Claims 72, 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi and Bencher as applied to claim 3 above, and further in view of the applicant's admitted prior art (AAPA).

With regard to claim 72, Takahashi and Bencher teach forming a photoresist over at least a portion of the anti-reflective layer. Takahashi and Bencher teach irradiating the photoresist. It is not clear if Takahashi and Bencher teach wherein the antireflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 70% or more. The AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein an antireflective layer reduces the reflectivity to a radiation that penetrates a photoresist by 70% or more. It would have been

obvious to use the antireflective layer of the AAPA in the method of Takahashi and Bencher in order to substantially reduce standing waves as stated by the AAPA on page 1, lines 23 – 24 and page 2, lines 1 – 6.

With regard to claim 73, the AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 71%.

16. Claims 75 and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma, Segawa, and Bencher as applied to claim 15 above, and further in view of the applicant's admitted prior art (AAPA).

With regard to claim 75, Kayanuma, Segawa, and Bencher teach forming a photoresist over at least a portion of the anti-reflective layer. Kayanuma, Segawa, and Bencher teach irradiating the photoresist. It is not clear if Takahashi and Bencher teach wherein the antireflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 70% or more. The AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein an antireflective layer reduces the reflectivity to a radiation that penetrates a photoresist by 70% or more. It would have been obvious to use the antireflective layer of the AAPA in the method of Kayanuma, Segawa, and Bencher in order to substantially reduce standing waves as stated by the AAPA on page 1, lines 23 – 24 and page 2, lines 1 – 6.

With regard to claim 76, the AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 71%.

17. Claims 78 and 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma, and Bencher as applied to claim 26 above, and further in view of the applicant's admitted prior art (AAPA).

With regard to claim 78, Kayanuma, and Bencher teach forming a photoresist over at least a portion of the anti-reflective layer. Kayanuma, and Bencher teach irradiating the photoresist. It is not clear if Takahashi and Bencher teach wherein the antireflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 70% or more. The AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein an antireflective layer reduces the reflectivity to a radiation that penetrates a photoresist by 70% or more. It would have been obvious to use the antireflective layer of the AAPA in the method of Kayanuma, and Bencher in order to substantially reduce standing waves as stated by the AAPA on page 1, lines 23 – 24 and page 2, lines 1 – 6.

With regard to claim 79, the AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 71%.

Response to Arguments

18. Applicant's arguments with respect to claims 15 – 30 have been considered but are moot in view of the new ground(s) of rejection.

19. Applicant's arguments filed December 11, 2002 have been fully considered but they are not persuasive.

20. With regard to the applicant's ascertation that "(specific reasons for the further rejection of claims 37 and 38 are not explicitly stated in the Office Action [dated 9-11-2002])." Attention is pointed to paragraph 22 of the office action dated September 11, 2002, and paragraph 14 above.

21. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "inter-plate undercutting") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Segawa et al ('785) is an English translation document of Segawa.

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
January 27, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800